

# SUMADOR – RESTADOR DE 8 BITS UTILIZANDO SUMADORES DE 2 BITS (FULL-ADDER) UTILIZANDO EL ESTILO ESTRUCTURAL.

```

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sumador_restador is
    Port ( a : in std_logic_vector(7 downto 0);
          b : in std_logic_vector(7 downto 0);
          s : out std_logic_vector(7 downto 0);
          carry : out std_logic;
          control : in std_logic);
end sumador_restador;

architecture estructural of sumador_restador is
--declaracion del componente a utilizar
component fulladder is
    Port ( Ci : in std_logic;
          A : in std_logic;
          B : in std_logic;
          Co : out std_logic;
          s : out std_logic);
end component;
--zona para crear las senales que usaremos para
--conectar los componentes
signal cob: std_logic_vector (7 downto 0);
signal acarreo: std_logic_vector (7 downto 0);
begin
zonal:    for i in 0 to 7 generate
            cob(i)<=control xor b(i);
        end generate zonal;
w:    fulladder port map (control,A(0),cob(0),acarreo(0),s(0));
zona2:  for i2 in 1 to 6 generate
            v:    fulladder port map (acarreo(i2-
1),A(i2),cob(i2),acarreo(i2),s(i2));
        end generate zona2;
z:    fulladder port map
        (acarreo(6),A(7),cob(7),acarreo(7),s(7));
        carry<=acarreo(7);
end estructural; library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sumador_restador is
    Port ( a : in std_logic_vector(7 downto 0);
          b : in std_logic_vector(7 downto 0);

```

```

        s : out std_logic_vector(7 downto 0);
        carry : out std_logic;
        control : in std_logic);
end sumador_restador;

architecture estructural of sumador_restador is
--declaracion del componente a utilizar
component fulladder is
    Port ( Ci : in std_logic;
          A : in std_logic;
          B : in std_logic;
          Co : out std_logic;
          s : out std_logic);
end component;
--zona para crear las senales que usaremos para
--conectar los componentes
signal cob: std_logic_vector (7 downto 0);
signal acarreo: std_logic_vector (7 downto 0);
begin
zonal:    for i in 0 to 7 generate
            cob(i)<=control xor b(i);
        end generate zonal;
w:    fulladder port map (control,A(0),cob(0),acarreo(0),s(0));
zona2:  for i2 in 1 to 6 generate
        v:    fulladder port map (acarreo(i2-
1),A(i2),cob(i2),acarreo(i2),s(i2));
        end generate zona2;
z:    fulladder port map
      (acarreo(6),A(7),cob(7),acarreo(7),s(7));
      carry<=acarreo(7);
end estructural;

```



aquí se toma como 256 - 256-6 y -7 respectivamente  
**S=251**

**Sumas normales**

**control = '0' el circuito se hace un sumador**

**Control='1' entonces el circuito se hace un restador**