

FULL ADDER

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity fulladder is
  Port ( Ci : in std_logic;
        A : in std_logic;
        B : in std_logic;
        Co : out std_logic;
        s : out std_logic);
end fulladder;

architecture ACS of fulladder is
  --la arquitectura en si, sera una ACS incondicional.
begin
  s<=A xor B xor Ci;
  Co<=(A and B)or (A and Ci) or (B and Ci);

end ACS;
```

