CONTADOR MÓDULO 16 CON CARGA PARALELA

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
entity contacarga is
port (clk,updown,clear,load:in std_logic;
          p    : in std_logic_vector (3 downto 0);
          q    : out std_logic_vector (3 downto 0));
end contacarga;
architecture algoritmo of contacarga is
begin
     process (clk,clear,load,p)
          variable temporal:std_logic_vector (3 downto 0);
          begin
          if load='1' then
          temporal:=p;
          elsif clear='1' then
          temporal:="0000";
          elsif clk='1' and clk'event then
               if updown='1' then
                    temporal:=temporal+1;
               else
                    temporal:=temporal-1;
               end if;
          end if;
          q<=temporal;
     end process;
end algoritmo;
```

USANDO EL TEST BENCH, SE OBTUVO LA SIGUIENTE SIMULACION